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ALL OPTICAL REVERSIBLE DATA DISTRIBUTOR

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Abstract:
Nowadays, It became the fashion among the researchers about creating the New Reversible Gates. In the Reversible Literature, already many gates are proposed but it is the first time to propose a Gate for a decoder(Data Distributor). The proposed GLG (Garbage Less Gate) has No Garbage output which denotes its power efficiency. In this paper 2:4 reversible decoder is constructed using GLG. The proposed gate is also extended to N:2N decoder using the proposed GLG Gate and the Fredkin Gate. The theoretical proposition is verified through Optisystem & Modelsim Software. A comparison with existing reversible decoders is also included.

Keywords:
Reversible Logic, Reversible Decoder, GLG Gate.

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1. INTRODUCTION

Reversible logic circuit synthesis is an introduction to design of quantum computing-based systems, low power CMOS circuits, and nanotechnology-based systems. Since quantum mechanics is essentially reversible, quantum mechanical processes appeared as good candidate to construct reversible gates and these gates are known as quantum gates [1]. After introduction of the idea of quantum computation it has already been seen that there exist some quantum algorithms [2] which work much faster than their classical counterparts, and these processes which establish quantum computing as a superior future technology involves quantum circuits and quantum gates. As quantum algorithms, quantum gates are more powerful than classical reversible gates [2]. There are some 3x3 classical reversible gates, provided constant inputs are permitted [3, 4]. On the other hand, major of quantum 2*2 gates are universal, without needing the constant inputs [1].

2. RELATED WORK

The authors had already proposed Universal Gate named ALL gate [5] which performs all the basic logical operation and also other Reversible gates named KTR [6] and SRM [7] which is used for the execution of the Full Adder and the Multiplexer.

- ALL Gate as Universal Gate

The 4*4 reversible ALL Gate [5] performs all the Basic Logical Operations like AND, OR, NOT, NAND, EXOR, EXNOR. It can be used for an ALU Design as it executes all the basic operations.

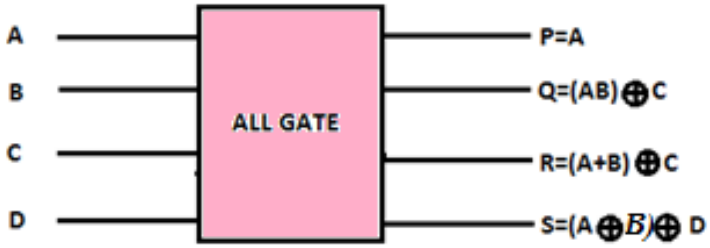

Fig. 1: Block Diagram of ALL GATE

The reversible ALL Gate is used to design all the logical operations as we have all the basic gates in the proposed ALL Gate. It is shown in the figure 1

- KTR Gate as Full Adder

The Reversible KTR Gate [6] acts as Full adder to exhibit the Sum and Carry when the input D is Supplied as '0' as shown in the figure 2. On Implementing KTR gate as a full adder we have 2 garbage outputs. Sum and Carry are taken in the output C and D respectively.

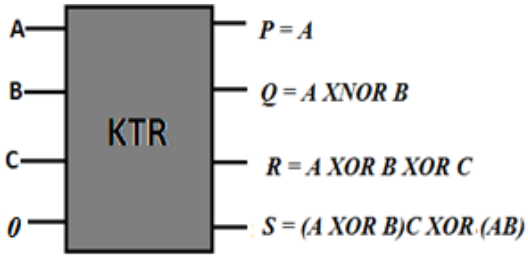

Fig. 2: Full adder using KTR Gate

- SRM Gate as Multiplexer

The inputs and the outputs of the proposed 3*3 reversible SRM Gate [7] are A, B, C and P, Q, R respectively. The simple block diagram of the proposed SRM Gate is shown in the figure 3.

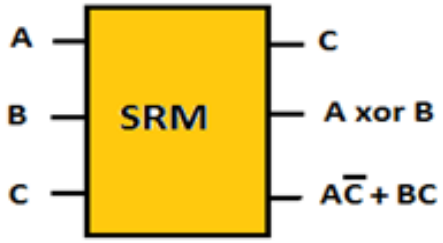

Fig. 3: Block Diagram of the SRM Gate

- Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B ⊕ AC and R=A′C ⊕ AB. Quantum cost of a Fredkin gate is 5. [13]

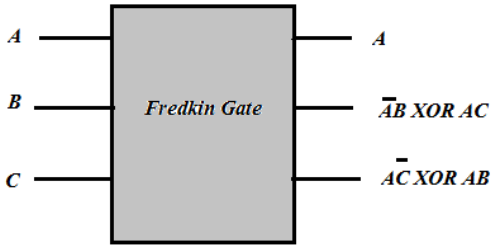

Fig. 4: Block Diagram of the Fredkin Gate

- SOA Based MZI

A photon can provide unmatched high speed and can store the information in a signal of zero mass. These properties of photon have attracted the attention of researchers to implement the reversible logic gates in all optical domain. In the recent years, researchers have implemented several reversible logic gates in optical computing domain such as Feynman gate, Toffoli gate, Peres gate and Modified Fredkin gate. The all optical implementation of reversible logic gates can be achieved using semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI) optical switches.

The Mach-Zehnder interferometer based implementation of reversible logic gates provides significant advantages such as high speed, low power, fast switching time, and ease in the fabrication. A design of all optical MZI switch is shown in Fig. 5. A MZI based all optical switch can be designed using two Semiconductor optical amplifier (SOA-1, SOA-2) and two couplers (C-1, C-2).The operating principle of MZI [14] based all optical switch can be explained as follows

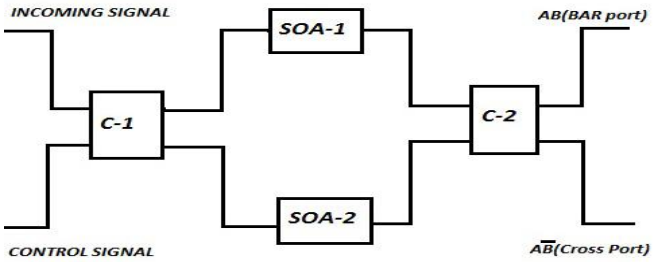

Fig. 5: SOA Based MZ1

In MZI there are two inputs ports A and B and two output ports called as bar port and cross port respectively, as shown in Fig.6. At the input ports, the optical signal coming at port B is considered as the control signal (λ2) and the optical signal coming at port A is considered as incoming signal (λ1). The working of the MZI can be explained as: (i) when there is an incoming signal at port A and the control signal at port B then there is a light present at the output bar port and there is no light present at the output cross port, (ii) in the absence of control signal at input port B and incoming signal at input port A then the outputs of MZI are switched and results in the presence of light at the output cross port and no light at the bar port. In this work, consider no light or absence of light is considered as the value 0. The above behavior of MZI based all optical switch can be written as Boolean functions having inputs to outputs mapping as (A, B) to (P=AB, Q = $\overline{AB}$), where A (incoming signal), B (control signal) are the inputs of MZI and P (Bar Port), Q (Cross Port) are the outputs of MZI, respectively. The block diagram of MZI based all optical switch is shown in Fig.6. In this work the optical cost and the delay (Δ) of MZI based all optical switch is considered as unity.

Fig 6: Mach-Zehnder Interferometer

3. PROPOSED WORK

- Introduction to the Garbage Less Gate (GLG)

The proposed GLG Gate is a 4 x 4 reversible gate. The inputs and the outputs be A, B, C, D and P, Q, R, S respectively.

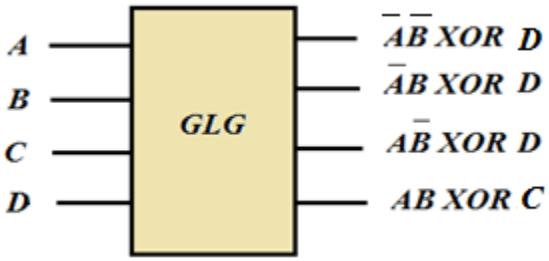

Fig. 7: Block Diagram of the GLG Gate

The proposed reversible GLG (Garbage Less Gate) Gate is used to design reversible $2:2^2$ Decoder. $2:2^2$ are implemented using a single GLG Gate.

- Truth Table of GLG

From the truth table it is clearly inferred that the proposed GLG is perfectly reversible as it is one to one mapping. The truth table is provided in table 1.

Table 1: Truth Table of the proposed Gate

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INPUT				OUTPUT			
A	*B*	*C*	*D*	*P*	*Q*	*R*	*S*
0	0	0	0	1	0	0	0
0	0	0	1	0	1	1	0
0	0	1	0	1	0	0	1
0	0	1	1	0	1	1	1
0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	0	1
0	1	1	1	1	0	1	1
1	0	0	0	0	0	1	0
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	1
1	0	1	1	1	1	0	1
1	1	0	0	0	0	0	1
1	1	0	1	1	1	1	1
1	1	1	0	0	0	0	0
1	1	1	1	1	1	1	0

- Decoder

A decoder is a combinational circuit used in many devices for processing [8]. It has multiple inputs as well as multiple outputs. Generally decoder is available as 2 to 4 decoder, 3 to 8 decoder, 4 to 16 decoder etc. A single Feynman gate can be used to design the basic *1 to 2* decoder.

- 2:4 Decoder using the proposed GLG

By using single GLG (Garbage Less Gate) the 2:4 Decoder were designed. Inputs A and B is given according to the block diagram and the input C and D is zero, the outputs are taken from

the P Q R and S output. Representation of the 2:4 Decoder. Using GLG Gate is given in the figure 8.

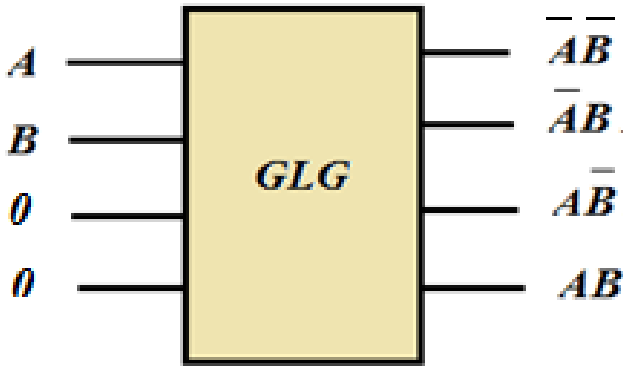


Fig. 8: Decoder Using GLG

- 3 : 8 Decoder using the proposed GLG

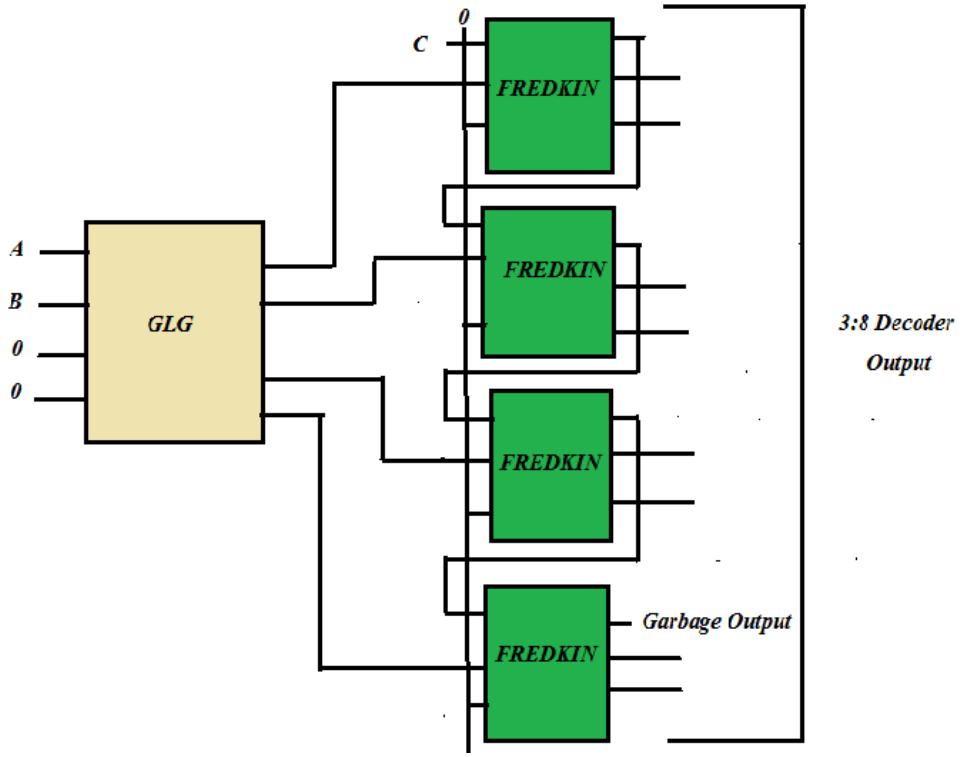


Fig. 9: 3:8 Decoder using the proposed GLG & Fredkin Gate

- Optical Implementation of the proposed GLG

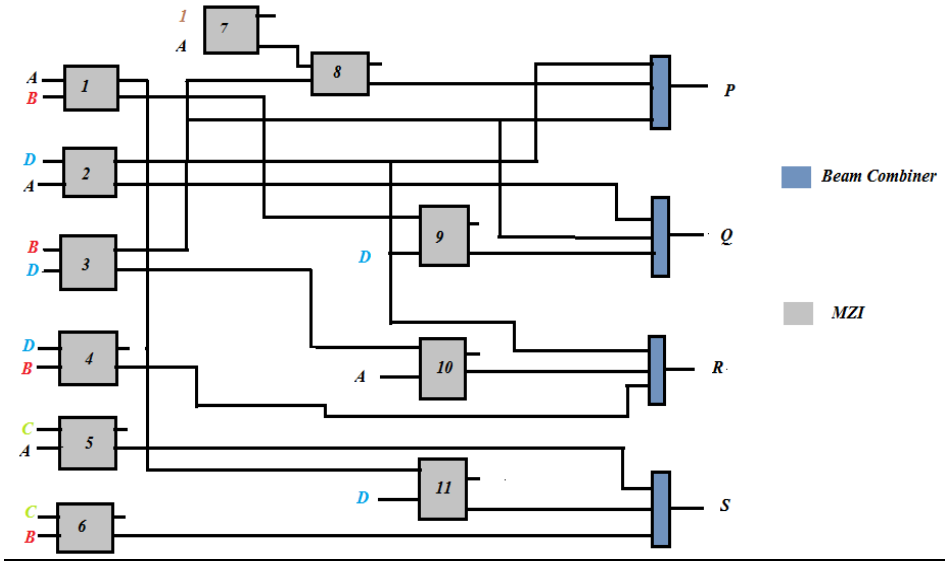


Fig. 10: Optical Implementation of the proposed GLG

Here we are using one GLG Gate and 4 Fredkin Gate to construct a 3:8 Decoder. It is very important to note that NOT Gate is the only one conventional logic gate which is Reversible as it possess one to one Mapping. As usual two inputs C and D is given as zero. The Inputs are given as A and B for GLG Gate. Then third Input is given in the second stage of the circuit. We can receive the output from the fredkin gate directly. The representation of the 3:8 decoder is shown in the figure 9.

- Truth Table of the 3 : 8 Decoder

The truth table of the proposed 3:8 Decoder, when the last input of the fredkin Gate is supplied as zero is given below.

Table 2: Truth Table of 3: 8 Decoder (S=0)

INPUTS			OUTPUTS							
A	B	E	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

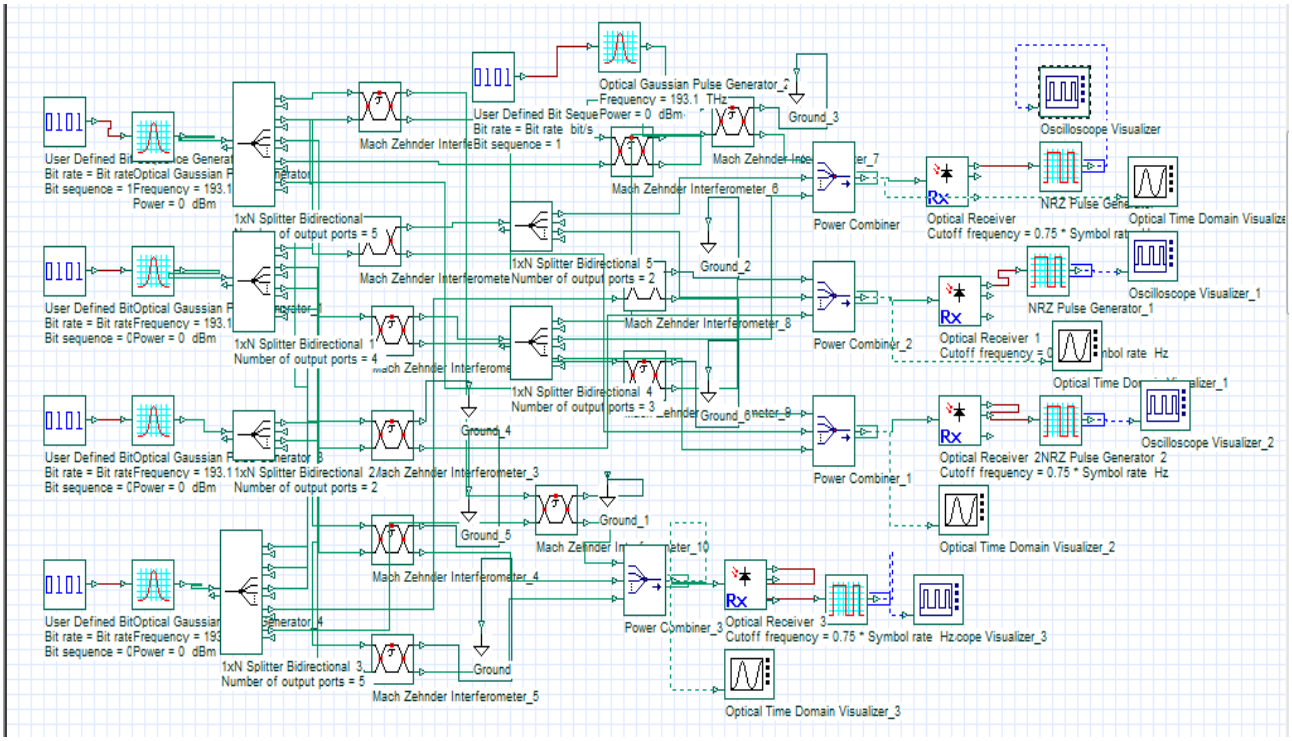
Table 3: Truth Table of 3: 8 Decoder (S=1)

INPUTS			OUTPUTS							
A	B	E	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

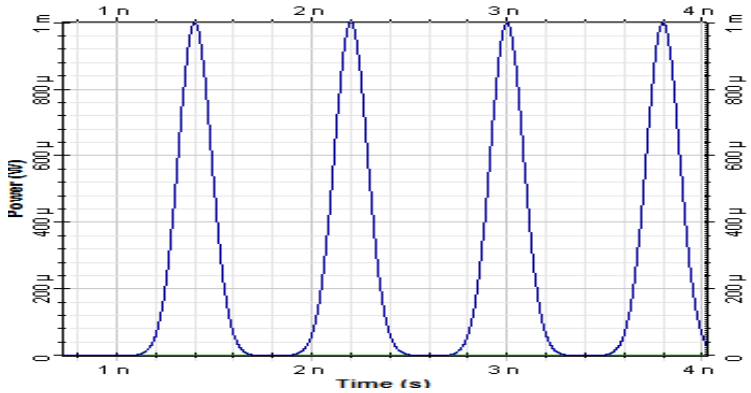
The truth table of the proposed 3:8 Decoder, when the last input of the fredkin Gate is supplied as one is given above.

4. SIMULATION RESULT

The circuit is also simulated using the Optisystem software. The optical implementation of the circuit is simulated and the output is verified.

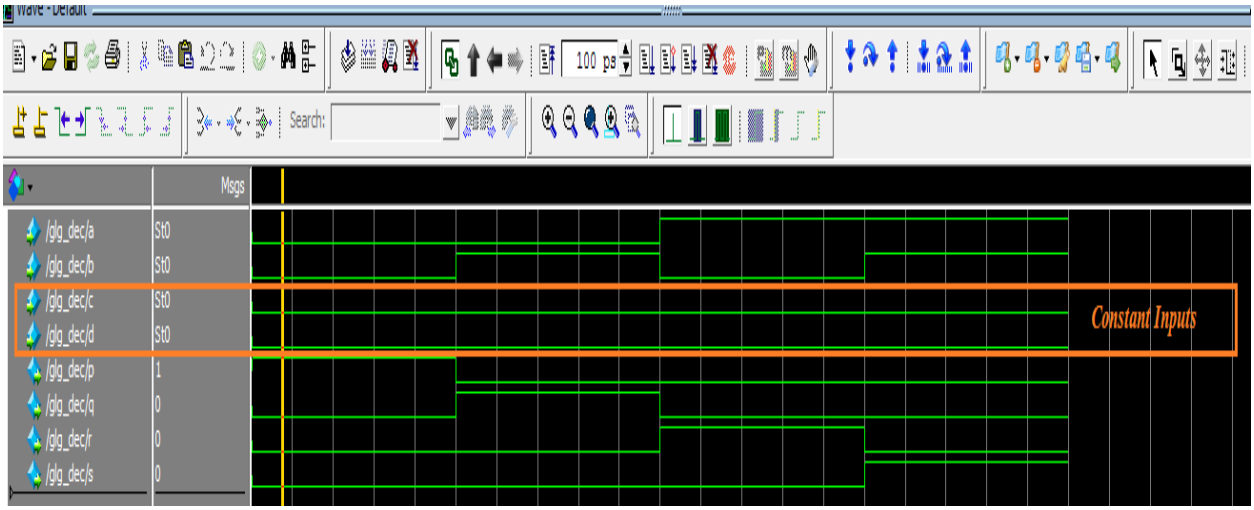


When A=0 B=0 (Constant Inputs C=0 & D=0) the A bar B bar gets Selected (P=1)

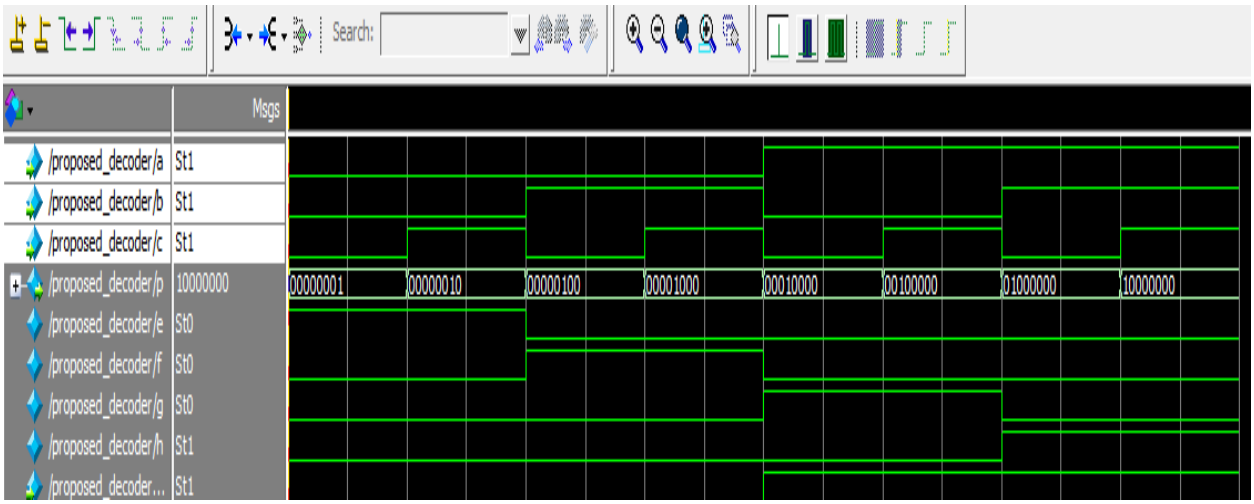


Similarly other outputs are verified.

The 2:4 Decoder is also simulated using the Modalism Software through the Verilog Code.



The 3:8 Decoder constructed by using GLG Gate and Fredkin Gate is simulated using the Modalism Software through the Verilog Code.



5. COMPARISON

The reason why we say the proposed Decoder is an efficient one as it has no Garbage Output only one Gate is used to execute the decoder. The proposed 2:4 decoder using GLG Gate is very efficient as shown in the chart 1.

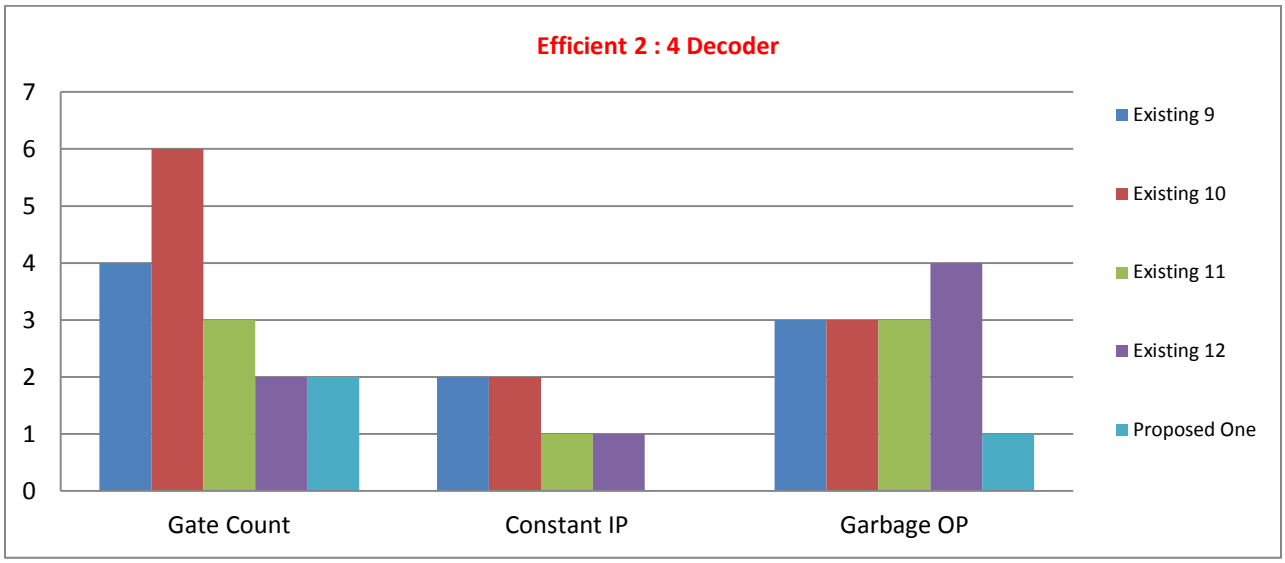


Chart 1: The proposed 2:4 decoder using GLG Gate

The proposed 3:8 decoder using GLG Gate and the NOT Gate is compared with the existing one [11], [12].

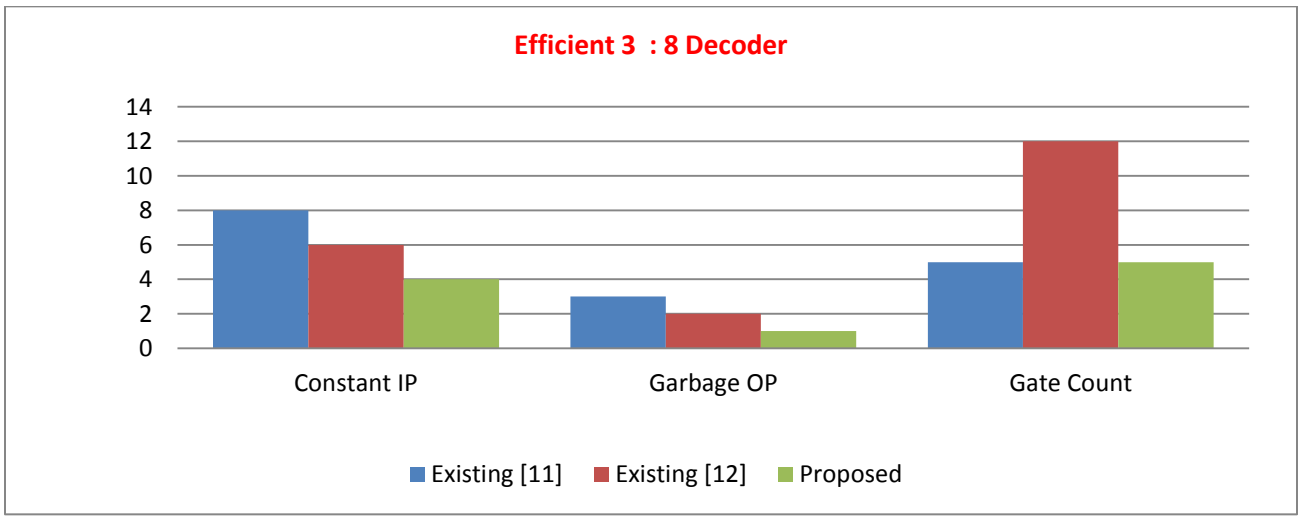


Chart 2: The proposed 3:8 decoder using GLG Gate and NOT Gate.

Also we can construct N: 2N Decoder using the proposed GLG Gate and the Fredkin Gate.

6. CONCLUSION

The drawback of any reversible digital circuit is high number of its gate count and the garbage output. This problem was overcome by the proposed design as it possesses only one gate and No Garbage Output. It is concluded that the proposed design is more efficient than the existing one.

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