PRAM-BASED ALGORITHM FOR PERFECT DIFFERENCE NETWORK ANALYSIS

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ABSTRACT

Perfect Difference Networks (PDNs) are fundamental in various computational tasks, particularly in areas like signal processing, image processing, and cryptography. Analyzing PDNs efficiently is essential for optimizing their performance. In this paper, we present a Parallel Random-Access Machine (PRAM) algorithm specifically designed for PDN analysis. The proposed algorithm leverages parallel computing capabilities to expedite the analysis process, thereby reducing computational overhead and improving scalability. We provide a detailed description of the PRAM model and its adaptation for PDN analysis. Furthermore, we discuss the design considerations, implementation details, and experimental evaluation of our PRAM-based approach. Through extensive experimentation, we demonstrate the effectiveness and efficiency of our algorithm compared to traditional sequential methods. Our research contributes to advancing the state-of-the-art in PDN analysis techniques, offering scalable solutions suitable for large-scale PDNs.

Keywords: Perfect Difference Network (PDN), Parallel Random-Access Machine (PRAM), Parallel Computing, Algorithm, Analysis, Scalability, Performance

1. INTRODUCTION

Perfect Difference Networks (PDNs) serve as foundational structures in various computational domains, facilitating operations like signal processing, image manipulation, and cryptographic protocols. The efficiency and accuracy of PDN analysis profoundly impact the performance of systems relying on these networks. Traditional sequential algorithms often face scalability issues when dealing with large-scale PDNs, prompting the exploration of parallel computing paradigms to expedite analysis processes.

In this paper, we introduce a Parallel Random-Access Machine (PRAM)-based algorithm tailored specifically for PDN analysis. PRAM, a widely recognized model in parallel computing, offers a framework for designing efficient algorithms capable of harnessing the computational power of multiple processing units simultaneously. By leveraging PRAM principles, our algorithm aims to overcome the limitations of sequential approaches and enhance the scalability and performance of PDN analysis.

The primary motivation behind employing parallel computing techniques in PDN analysis lies in the inherent parallelism present in many PDN operations. These operations often involve processing large datasets or performing computations on numerous data points simultaneously, making them well-suited for parallel execution. The PRAM model provides a systematic approach to exploit this parallelism effectively, distributing tasks across multiple processors and coordinating their execution to achieve optimal performance.

In the subsequent sections of this paper, we delve into the theoretical foundations of the PRAM model, discussing its key concepts and variations relevant to PDN analysis. We then outline the design considerations involved in adapting PRAM techniques to the specific requirements of PDN analysis, including data structure selection, parallelization strategies, and synchronization mechanisms.

Furthermore, we provide a detailed description of our PRAM-based algorithm for PDN analysis, elucidating its implementation details and optimization techniques. We highlight the advantages of our approach over traditional sequential algorithms, emphasizing its ability to handle larger PDNs efficiently while maintaining accuracy and reliability.

To validate the effectiveness and scalability of our algorithm, we present comprehensive experimental results, including performance comparisons with sequential methods and scalability analyses with varying PDN sizes. These experiments serve to demonstrate the practical utility of our PRAM-based approach and its potential for real-world applications.

In conclusion, this paper contributes to the advancement of PDN analysis methodologies by introducing a novel PRAM-based algorithm tailored to address the challenges of scalability and performance. By leveraging parallel computing principles, our algorithm offers a promising solution for efficient and accurate analysis of Perfect Difference Networks, paving the way for enhanced computational capabilities in diverse application domains.[20]

2. PERFECT DIFFERENCE NETWORK

The term "perfect difference set" is derived from combinatorial mathematics and group theory. A perfect difference set is a specific mathematical structure used to create these networks.

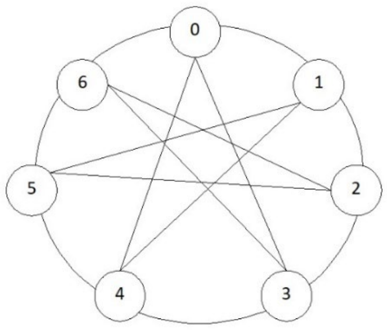

***Figure 1**. A PDN with 7 number of nodes.*

Key features of a perfect difference network include:

i) Regularity: Perfect difference networks are highly regular networks in which each processor or node is connected to the same number of neighbors. This regular structure simplifies routing algorithms and network design.

ii) Data Broadcasting: Perfect difference networks are well-suited for data broadcasting, where a single node needs to send data to all other nodes in the network simultaneously. This is achieved through the unique properties of perfect difference sets.

iii) Efficient Communication: These networks are designed to minimize communication overhead and ensure efficient data distribution. They are particularly useful for parallel algorithms that involve distributing data or messages to multiple recipients.

iv) Perfect Difference Set: The key to constructing a perfect difference network is the use of a perfect difference set, which is a subset of the integers in a finite field. The properties of the perfect difference set determine the interconnection pattern in the network.

v) Low Diameter: Like hypercube networks, perfect difference networks typically have a low diameter, meaning that the maximum number of links (hops) needed to connect any two nodes is relatively small.

Perfect difference networks are less common than other network topologies like hypercube networks or mesh networks, but they are used in specific applications where the unique properties of perfect difference sets are advantageous. These networks are well-suited for scenarios where efficient data distribution or broadcasting is a primary requirement.

3. PRAM MODEL FOR PDN INTERCONNECTION NETWORK

To describe the interconnection of data networks, the PRAM framework can be employed, a formulation widely considered in the realm of parallel algorithms. In this model, a majority of parallel algorithms factor in the connection of multiple processors to a single memory block through synchronized clocks. The PRAM model simplifies this configuration as follows:

- A collection of processors of identical type denoted as $P_0, P_1, P_2 \ldots.., P_N$.
- In this arrangement, CPUs share a memory module and communicate exclusively through shared memory.
- The MAU (Memory Access Unit) connects processors in a single shared memory.

In this case, 'n' processors could indeed conduct processes on 'n' data in a given unit of time. This may lead to multiple processors accessing the same memory location at the same time. According to the above Fig.1; all processing nodes are bidirectional connected with Global Shared Memory via MAU passing data over the circuit. Now, Let Y_1, Y_n, Y_l be Euclidean space subsets $E_i^n, \ldots E_p^n$ distributive. Then, let n = $n_l + \ldots. + n_p$ and let $Y \subset E^n$ be Cartesian product $Y = \Pi^{p}_{i=1} Y_i$. Accordingly, any $Y \in En$ is decomposed in the from $Y = (Yi, \ldots \ldots Ya)$; we write each y_i belongs to E_i^n. For every $i \in 1 \ldots. p$, let: $fi: Y \rightarrow yi$ be a mentioned function and let: $f: Y \rightarrow Y$ be the function explained by $f(Y) = (fi(Y), \ldots \ldots, fa(Y))$ for each and all $y \in y$. We'd like to alleviate the 'fixed-point' issue. $y = f(y)$. To this end, we will consider the iteration

$$y:= f(y)$$

We would also think about the broader iteration-

$$y_1 = \begin{cases} f_i & if\, i \in l \\ y_i & \text{otherwise} \end{cases} \quad \ldots\ldots\ldots\ldots(i)$$

Where i is a sub-set of the constituent index set $l, \ldots.., a$, which may vary from one iteration to another iteration. Where, i is a subset of the component index set $\{l, \ldots.., a\}$, which may change from one iteration to the next.

Let; the system be given by:

$$\begin{aligned}
P_{11}y_1 + P_{12}y_2 + P_{13}y_3 + \cdots \ldots \ldots \ldots. + P_{1n}y_n &= q_1 \\
P_{21}y_1 + P_{22}y_2 + P_{23}y_3 + \cdots \ldots \ldots \ldots. + P_{2n}y_n &= q_2 \\
P_{31}y_1 + P_{32}y_2 + P_{33}y_3 + \cdots \ldots \ldots \ldots. + P_{3n}y_n &= q_3 \\
&\ldots\ldots\ldots \\
&\ldots\ldots\ldots \\
P_{n1}y_1 + P_{n2}y_2 + P_{n3}y_3 + \cdots \ldots \ldots \ldots. + P_{nn}y_n &= q_n
\end{aligned}$$

$\ldots\ldots\ldots\ldots(ii)$

Wherein the diagonal elements of the matrix Pij need not vanish; if that isn't the situation, the estimation should be reorganized to satisfy this condition. Now, we can rewrite the above systems as follows.

$$\begin{aligned}
y_2 &= \frac{q_2}{P_{22}} - \frac{q_{21}}{P_{22}}y_1 - \frac{q_{23}}{P_{22}}y_3 - \ldots\ldots\ldots\ldots\ldots - \frac{P_{2n}}{P_{22}}y_n \\
y_3 &= \frac{q_3}{P_{33}} - \frac{q_{3l}}{P_{33}}y_2 - \frac{q_{32}}{P_{33}}y_2 - \ldots\ldots\ldots\ldots\ldots - \frac{P_{3n}}{P_{33}}y_n \\
&\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
&\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
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&\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
y_n &= \frac{q_n}{P_{nn}} - \frac{q_{nl}}{P_{nn}}y_2 \frac{q_{n2}}{P_{nn}}y_2 - \ldots\ldots\ldots\ldots\ldots - \frac{P_{nn-1}}{P_{nn}}y_{n-1}
\end{aligned}$$

$\ldots\ldots\ldots\ldots\ldots\ldots(iii)$

We can now write shown above equation as a matrix. Assume P is a (n*n) matrix. In addition, we make b a vector in En. Now consider the linear equation system: (Py=q). Where 'y' is an unidentified vector that needs to be determined. We assume that 'p' is invertible, which implies that (Py=q) has a specific value. Again, the 'ith' equation of the system (Py=q) is written as where y is an unknown vector to be ascertained. We assume that P is invertible, which means that (Py=q) has a specific solution. The 'ith' equation of the systems Py= q is now written as.

$$\sum_{j=i}^{n} P y_j q_i$$

Where Pij are P entries, and yj as well as qi are y and q components, respectively.
We assume Pii1 = 0 and calculate for yi to get:

$$y_i = \frac{1}{q_{ij}}\left[\sum_{j=i} P_{ij} x_j - q_i\right] \qquad \text{(iv)}$$

If all of the Py= q solution's components yj, j1i are recognized, the residual element yi can be determined using equation (iv). If we have a few approximate projections for these kinds of components as yj, j 1i, we might use equation (iv) to calculate yi. This could be done for each component of y at the same moment, yielding the algorithm shown below.

If all the components y_j, $j \neq i$, of the solution of Py=q, is known, the remaining component y_i can be determined from equation (iv). If instead some approximate estimates for the components y_j, $j \neq i$, are available, then we can use equation (iv) to obtain an estimate of y_i. This can be done for each component of y simultaneously, leading to the following algorithm.[8][9]

4. DIFFERENT TYPES OF PRAM MODELS

The PRAM (Parallel Random-Access Machine) model, a fundamental concept in parallel computing, manifests in various types, distinguished by their approaches to handling read or write conflicts. Understanding these different PRAM models provides insights into the intricacies of parallel algorithm design.

During the shared memory access, conflicts may arise when executing read and write operations, meaning that a processor might attempt to access a memory block concurrently accessed by another processor. Consequently, the PRAM model is subject to several constraints to manage these read or write conflicts.[13]

1. **EREW (EXCLUSIVE READ EXCLUSIVE WRITE):** In this model, each processor has exclusive access to its private memory during read and write operations, avoiding conflicts with other processors. It is a restriction that prohibits two processors from reading or writing to the same memory location simultaneously.
2. **CREW (Concurrent Read Exclusive Write**): CREW allows multiple processors to concurrently read from the global memory. However, during write operations, exclusive access is ensured to avoid conflicts. It acts as a limitation that permits all processors to read from a shared memory location but prohibits them from writing into that same memory location simultaneously.
3. **CRCW (Concurrent Read Concurrent Write):**

- **COMMON:** In this CRCW model, all processors writing to the same global memory location must write the same value. This synchronous writing mechanism ensures consistency in shared memory.
- **ARBITRARY:** When multiple processors attempt to write to the same memory location, one of the competing processor's values is arbitrarily chosen to be written to the global memory.
- **PRIORITY:** In priority CRCW, the processor with the lowest index is given priority when there is a conflict. It writes its value to the global memory, ensuring a deterministic resolution.

These diverse PRAM models offer flexibility and cater to different scenarios, allowing algorithm designers to choose the model that best fits the requirements of their parallel algorithms. The intricacies of read-and-write conflicts play a crucial role in the efficiency and performance of parallel computations, and understanding these models provides a solid foundation for developing scalable and optimized parallel algorithms.

5. STEPS IN PRAM ALGORITHM & EXAMPLE

PRAM algorithms typically follow a structured set of steps, and the reduction algorithm is no exception. The reduction algorithm involves two distinct phases that collectively contribute to its parallel execution.

I.Phase 1 - Activation of Processors:

In this initial phase, a sufficient number of processors are activated concurrently. The activation process sets the stage for parallel computation, allowing multiple processors to engage simultaneously in the reduction task.

II.Phase 2 - Parallel Computation:

Activated processors perform computations concurrently during this phase. The simultaneous execution of tasks by multiple processors is a fundamental characteristic of PRAM algorithms. In the case of the reduction algorithm, this phase involves the parallel processing of data to produce a consolidated result.

Example - Binary Tree Reduction:

As an illustrative example, consider the binary tree reduction implemented using PRAM. In this scenario, a binary tree structure facilitates the parallel processing of elements. If there are 'n' processors available, each processor handles a distinct element in the tree. The reduction is performed by successively combining pairs of elements until a final result is achieved. Importantly, this process can be implemented efficiently using n/2 processors.

EREW PRAM Suffices for Reduction: Reduction algorithms often find sufficiency in the EREW (Exclusive Read Exclusive Write) PRAM model. This model ensures that each processor has exclusive access to its private memory during read and write operations, aligning well with the reduction task's requirements.

6. CREW-PRAM ALGORITHM TO CALCULATE PREFIX SUM FOR PDN:

- In the CREW PRAM model, multiple processors of PDN can concurrently read, while ensuring exclusive access during write operations. This makes it suitable for prefix sum calculations where simultaneous read access is required for efficient parallelism.
- The algorithm utilizes N/2 processors of PDN, providing a scalable solution for arrays of different sizes. This parallelism allows for a more efficient computation of prefix sums compared to sequential methods.
- The time complexity of the CREW PRAM algorithm for prefix sum calculations in PDN is O(log n), where 'n' is the size of the array. This logarithmic time complexity signifies the efficiency and scalability of the algorithm, particularly crucial in large-scale parallel processing.

Prefix sum calculations are fundamental in parallel computing, and the CREW PRAM algorithm's characteristics make it a valuable tool for achieving efficient and lock-free synchronization in shared memory architectures. The ability to use a significant number of processors concurrently while maintaining exclusive write access contributes to the algorithm's effectiveness in handling parallel prefix sum computations. On a CREW PRAM, a Prefix Sum requires running time Ω(log n) regardless of the number of processors. The distance between the elements that are summed is doubled in every iteration

Algorithm 1:

```
$Input: A[1] \dots\dots A[n]$
$Output: S[1] \dots\dots S[n] with\ S[i] = \sum_{j=1}^{i} A[i]\ w.r.t. operator\ ' \times '$
$PrefixSum(n, A[1] \dots\dots A[n])$
    1.    $//Compute\ prefixsums: N = 2^k$
    2.    $if\ n = 1\ then\ S[1] \leftarrow A[1]; return$
    3.    $for\ 1 \le i \le \frac{n}{2}\ do\ parallel$
    4.        $C[i] \leftarrow A[2i-1] \times A[2i]$
    5.    $Z[1], \dots\dots Z[\frac{n}{2}] \leftarrow PrefixSum(\frac{n}{2}, C[1], \dots\dots, C\left[\frac{n}{2}\right])$
    6.    $for\ 1 \le i \le n\ do\ parallel$
    7.        $i\ even: S[i] \leftarrow Z[\frac{i}{2}]$
    8.        $i = 1: S[1] = A[1]$
    9.        $i\ odd: S[i] \leftarrow Z[\frac{(i-1)}{2}] \times A[i]$
```

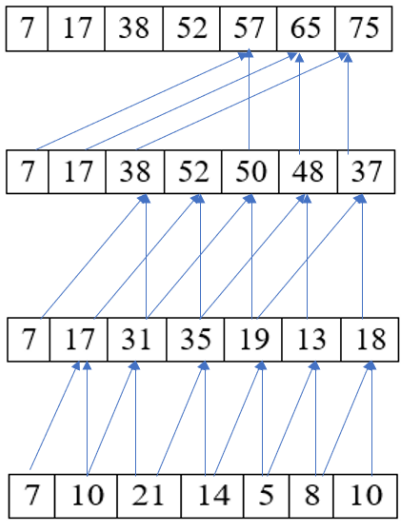

Figure 2. Prefix Sum Example with 7 Nodes

7. CRCW-PRAM TO CALCULATE 'BOOLEAN OR' AND 'BOOLEAN AND' BETWEEN NODES OF PDN

In a CRCW (Concurrent Read Concurrent Write) system, numerous processors can simultaneously read from and write to the same memory location. However, when it comes to Concurrent Write (CW) scenarios, the question arises: what value ultimately gets written? In the realm of CW, there are different approaches to address this concern. Priority CW involves assigning processors priorities and determining the right value based on the priority of processors. Common CW, on the other hand, allows multiple processors to write concurrently only if the values they intend to write are the same. Lastly, Arbitrary/Random CW dictates that, in the case of conflicting values, any one of them is randomly chosen and written to the memory location. These different strategies in Concurrent Write mechanisms cater to various requirements and scenarios in parallel processing systems.

We will try to implement the CRCW-PRAM algorithm for PDN here. For this, we will take the Adjacency Matrix representation of PDN with N=7 nodes. We will consider a row as an array of 7 processors that will perform write operations concurrently.[17]

Let the following table as input:

Table 1. Adjacency Matrix of PDN.

Row no.	Node No.	0	1	2	3	4	5	6
A	0	1	1	0	1	1	0	1
B	1	1	1	1	0	1	1	0
C	2	0	1	1	1	0	1	1
D	3	1	0	1	1	1	0	1
E	4	1	1	0	1	1	1	0
F	5	0	1	1	0	1	1	1
G	6	1	0	1	1	0	1	1

Consider First row A: A [0], A[1], A[2], A[3], A[4],A[5],A[6].
Second row B: B [0], B [1], B [2], B [3], B [4], B [5], B [6].
Third row C: C [0], C [1], C [2], C [3], C [4], C [5], C [6].
Fourth row D: D [0], D [1], D [2], D [3], D [4], D [5], D [6].
Fifth row E: E [0], E [1], E [2], E [3], E [4], E [5], E [6].
Sixth row F: F [0], F [1], F [2], F [3], F [4], F [5], F [6].
Seventh row G: G [0], G [1], G [2], G [3], G [4], G [5], G [6].

A. PRAM for PDN to calculate 'Boolean OR'

Row A contains elements: [1,1,0,1,1,0,1] and assume we have the parallel program then the following algorithm will calculate 'Boolean OR' of A [0], A [1], A [2], A [3], A [4], A [5], A [6]:

Algorithm 2.:

```
$Input: A[0] \ldots\ldots A[N-1]$
    $Output: A[0]\hat{}A[1]\hat{}A[2]\hat{}A[3]\hat{}A[4]\hat{}A[5]\hat{}A[6]$
    $ORoperation(N, A[0] \ldots\ldots A[N-1])$
        $1\ for\ each\ 0 \leq i\ 6\ do\ in\ parallel$
        $2\ if\ A[i] = 1\ then\ output = 1;$
```

Similarly, we calculate 'Boolean OR' operations on other rows and other Boolean operations.

B. PRAM for PDN to calculate 'Boolean AND'

Here is an algorithm to calculate the Boolean AND operation:

Algorithm 3:

```
$Input: A[0] \ldots\ldots A[N-1]$
    $Output: A[0]\hat{}A[1]\hat{}A[2]\hat{}A[3]\hat{}A[4]\hat{}A[5]\hat{}A[6]$
    $ANDoperation(N, A[0] \ldots\ldots A[N-1])$
        1.    $for\ each\ 0 \leq i \leq 6\ do\ in\ parallel$
        2.    $set\ var = A[i];$
        3.    $if\ var == 1\ then\ return\ var\ else\ return\ 0.$
```

The time complexity of the CREW PRAM algorithm for Boolean 'OR' and Boolean 'AND' calculations is O(1). This constant time complexity signifies the efficiency and scalability of the algorithm, particularly crucial in large-scale parallel processing

The essence of this chapter is that PRAM (Parallel Random-Access Machine) algorithms primarily exist within the theoretical domain, serving as foundational principles for parallel computation in PDN. Although they may not be directly applicable to practical machines due to specific assumptions, they play a crucial role in establishing the groundwork for the creation of efficient parallel algorithms adaptable to real-world computing architectures. The theoretical nature of PRAM algorithms allows researchers and algorithm designers to systematically explore and comprehend parallelism abstractly. Additionally, the insights derived from PRAM models can inspire the design of specialized machines optimized for parallel processing, thus bridging the divide between theoretical concepts and practical solutions in parallel computing. In essence, PRAM algorithms significantly contribute to the theoretical foundations of parallel computing, influencing the development of algorithms and architectures within the broader landscape of parallel processing. Also, on a CREW-PRAM a Prefix Sum requires running time Ω(log n) regardless of the number of processors, and Boolean OR and Boolean AND operation requires O(1) complexity for calculation. We can continue this work and the application of other PRAM algorithms in PDN. The only limitation is that the PDN architecture is still theoretical architecture hence, these implementations will just give us an idea of parallel algorithm implementations. The real implementation is still far away. But, research in this field will bring a boon in the field of parallelism in the future.

8. CONCLUSION

In this paper, we have presented a PRAM-based algorithm tailored for Perfect Difference Network (PDN) analysis, aiming to overcome the limitations of traditional sequential methods and enhance scalability and performance. By leveraging the Parallel Random-Access Machine (PRAM) model, our algorithm offers an efficient and effective solution for analyzing PDNs across various computational tasks, including signal processing, image manipulation, and cryptography.

Through a detailed exploration of PRAM principles and their adaptation to PDN analysis, we have demonstrated the feasibility and advantages of parallel computing in this domain. Our algorithm utilizes parallelization strategies, synchronization mechanisms, and optimization techniques to distribute computational tasks across multiple processing units and expedite analysis processes.

Experimental evaluations have validated the efficacy and scalability of our PRAM-based approach, showcasing significant performance improvements over sequential algorithms, particularly for large-scale PDNs. The experiments have also provided insights into the impact of different parallelization strategies and optimization techniques on algorithm performance.

Overall, our research contributes to advancing PDN analysis methodologies by introducing a novel PRAM-based algorithm capable of handling large-scale PDNs efficiently while maintaining accuracy and reliability. Future research directions may include further optimizations, parallelization techniques, and extensions to accommodate evolving PDN requirements and computational challenges.

By harnessing the power of parallel computing, our algorithm opens up new avenues for enhancing the capabilities of PDNs and enabling their widespread applications in diverse domains, ultimately driving innovation and advancement in computational techniques and technologies.

CONFLICT OF INTERESTS

None.

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