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A 6-BIT HIGH SPEED ANALOG TO DIGITAL CONVERTER USING INTEL 8085 MICROPROCESSOR

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ABSTRACT

Architecture to simplify the circuit implementation of the analog-to-digital (A/D) converter is proposed, the approach partitions input range into N-quantization cells, separated by N-1 boundary points. The Microprocessor decides with in which cell the input sample lies. The successive approximation technique translates input sample to digital domain. This makes the quantization feasible with much higher speed than with conventional successive approximation technique. Results of 8 bit prototype is presented.

Keywords: Quantization, Analog-to-Digital, Microprocessor

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1. INTRODUCTION

Analog-to-Digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2^{N-1} comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2].

All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially, consequently and this architecture requires very large IC's. It has high power dissipation.

The conventional pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed trade-offs between speeds, power consumption and die area [3]-[5]. Among a variety of pipelined ADCs, the multi bit-per-stage architecture is more suitable for high resolution, as the single bit-per stage structure requires more stages, high power consumption and larger chip area [6]. However the multi bit-per-stage architecture has a

relatively low signal processing speed due to reduced feedback factor in the closed loop configuration of the amplifiers. In switched capacitor type multiplying Digital-to-Analog converters (MDACS) used in conventional pipelined ADCs, the mismatch between capacitors limits the differential non linearly (DNL) of ADCs. This is because each DNL step is defined by the random process variation of each unit capacitor value. A common centroid geometry layout technique can improve this capacitor matching for DNL, but it cannot have an effect on random mismatch [7]. Naturally increasing the capacitor size can directly improve the capacitor matching accuracy, but at the added cost of increased load capacitance. This means the amplifiers would dissipate more power or the ADC sampling speed would be reduced.

In this paper, a novel architecture is proposed to improve the sampling rate and the resolution of an ADC. The prototype ADC based on this technique needs only four comparisons instead of eight comparisons normally required in the conventional successive approximation techniques for 8-bit resolution. This can increase the speed of conversion. This paper is organized as follows: The ADC architecture with the proposed technique is discussed in section I. Circuit implementation is described in Section III and measured results of the prototype are summarized in Section IV. Finally, the conclusions have been discussed in Section V.

2. ADC ARCHTECTURE

The block diagram of the proposed 8-bit ADC is illustrated in Figure 1. It is based on a conventional successive approximation technique. The ADC consists of an input sample and hold amplifier (SHA), 8-comparators, one 6-bit DAC, 8-bit microprocessor 8085 and some extra supporting circuit blocks. Seven comparators, partitions input range into 8-quantizaion cells. The microprocessor divides within which cell the input sample lies. This gives three MSB bits 000 to 111 according to the cell value. Remaining three bits are obtained by successive approximation technique.

A circuit which partitions Analog input signal into 8-quantization cells as shown in Figure 2, has seven comparators and a potential divider network. During sampling all comparators samples the analog input voltage V_{in} simultaneously and generates thermometer code. A binary count is loaded into the accumulator depending on the thermometer code, the detailed binary count loaded into accumulator for different thermometer code is summarized in Table-1.

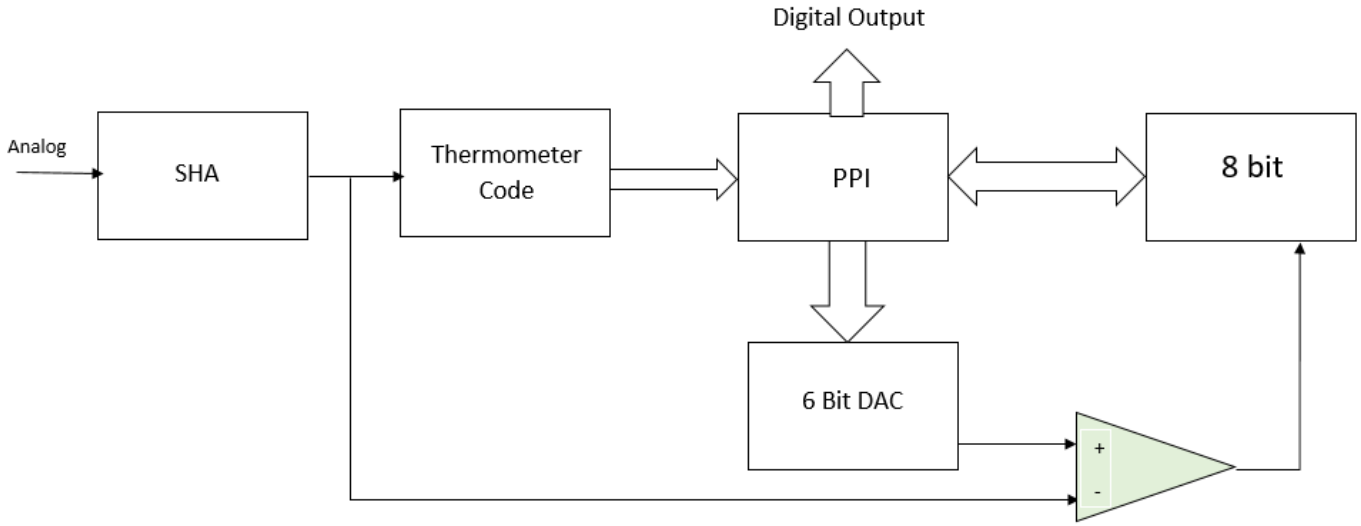

Figure -1 Block Diagram of 8 bit ADC

3. MICROPROCESSOR

The analog to digital converter is designed and developed using Intel 8085 microprocessor, it is a 8 bit NMOS general purpose microprocessor capable of addressing 64k of memory. It is a 40 pin IC package fabricated on a single LSI chip. The device requires a +5V single power supply and can operate with a 3MHz single phase clock. The clock cycle is of 320nS. The time for the clock cycle of the Intel 8085 is 200nS. It has 80 basic instructions and 246 op codes [8]

Thermometer Code	Count to be loaded
0000000	000100

0000001	001100
0000011	010100
0000111	011100
0001111	100100
0011111	101100
0111111	110100
1111111	111100

Table 1: Binary Count Corresponding to thermometer code

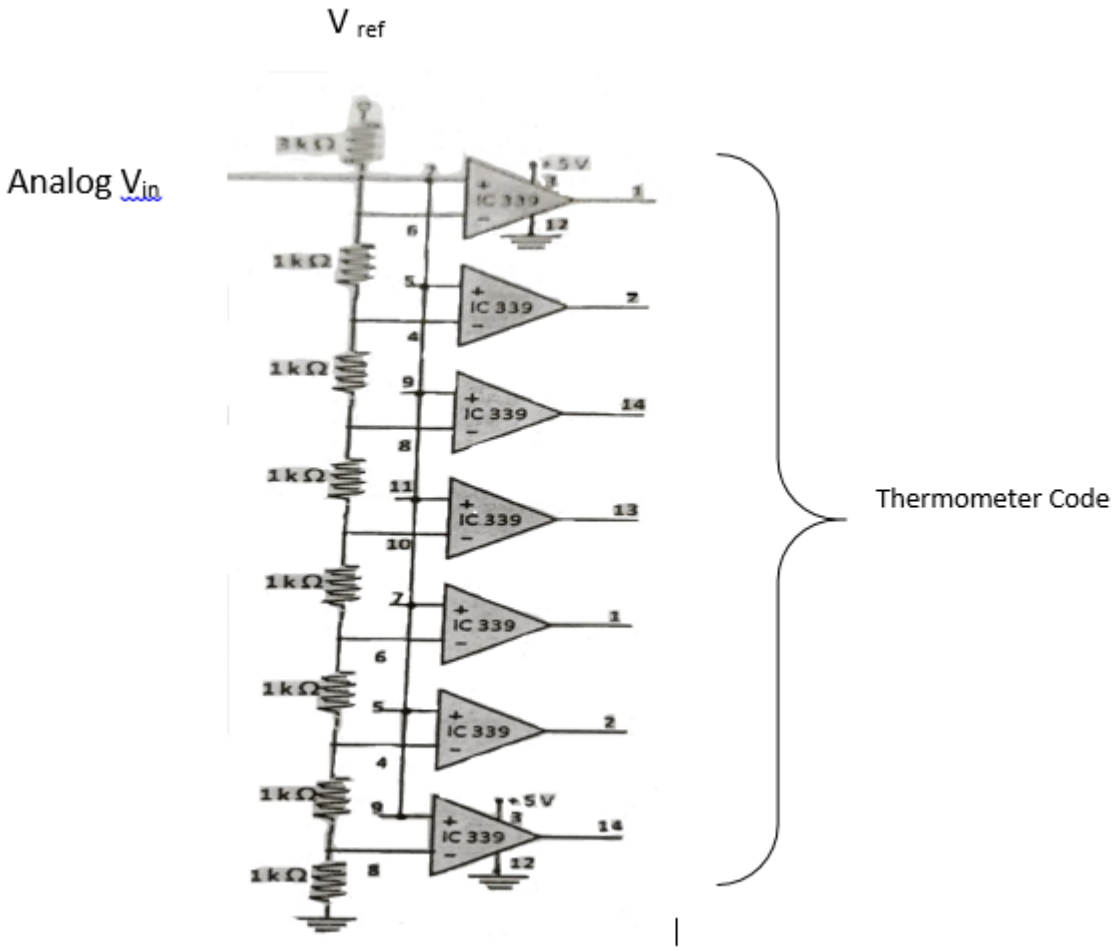

Figure 2: Thermometer code generator

4. PPI 8255

PPI 8255 is a programmable Peripheral Interface (PPI). Its main functions are to interface peripheral devices to the microcomputer. It has three 8 bit ports, namely port A, port B and port C, the port C is further divided into two 4 bit ports, port C upper and port C lower. Each port can be programmed as either an input port or output port [9].

The thermometer code generated by comparator network is fed to the PPI 8255. Depending on the thermometer code a binary count is loaded in an accumulator of the microprocessor as given in table 1. The successive approximation technique is used to get a digital code for the analog signal.

The PPI 8255 port A is used as input port which gets the thermometer code from comparator network. Port B is used as output port connected to 6-bit DAC to obtain analog signal equivalent to digital count in an accumulator, which is

compared with an analog input voltage V_{in}. After completion of four comparisons, count in the accumulator is digital equivalent of analog input voltage V_{in}.

Software:

The software for the Analog to Digital conversion is written in assembler codes and converted to hexadecimal code by the assembler software. Hex codes are transferred to the Microprocessor by a programmer. State diagram or the flow chart of the ADC is shown in figure 3.

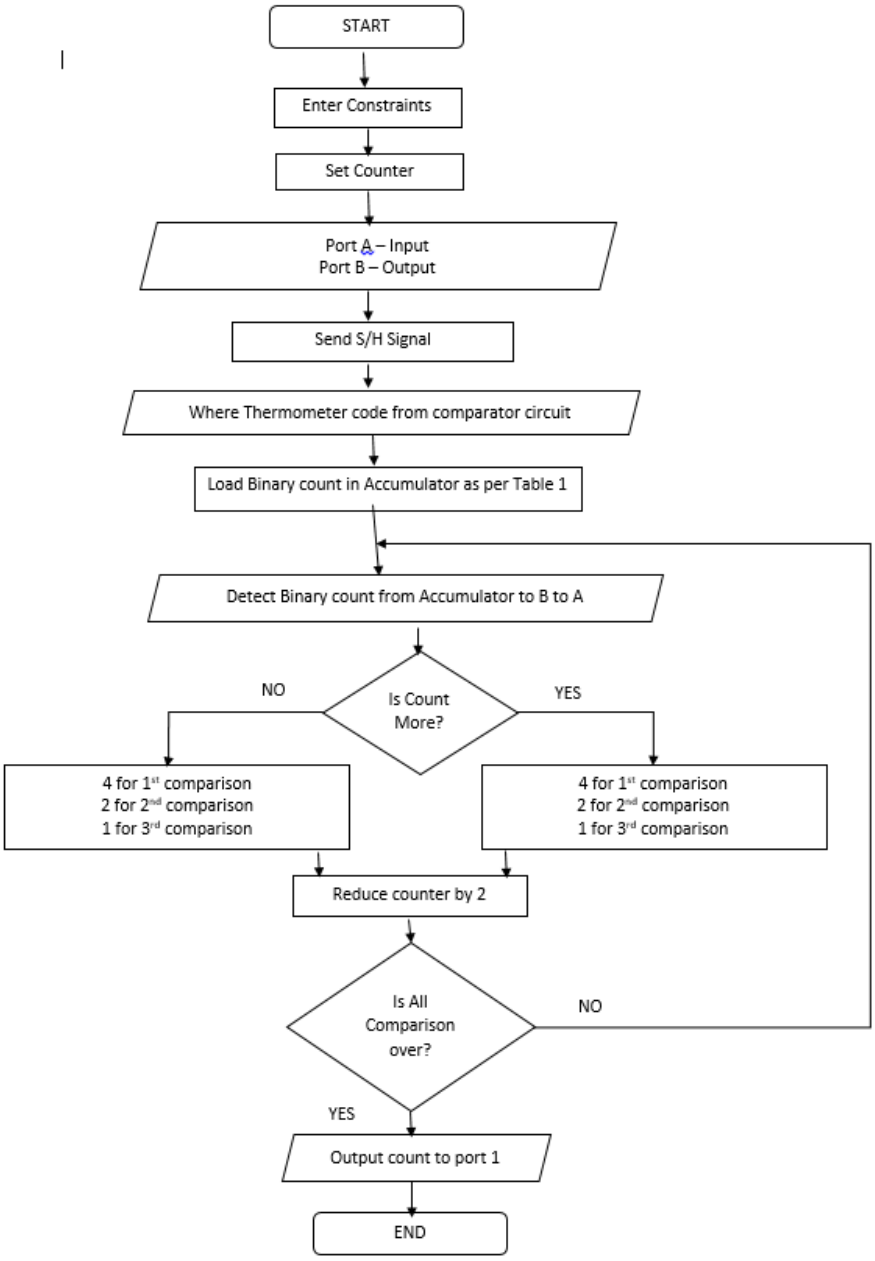

Figure 3: State Diagram

5. EXPERIMENTAL RESULTS:

Figure 4 shows the DC Linearity of the ADC. In figure 4(a) differential nonlinearity (DNL) is plotted versus code, and in Figure 4(b) integral nonlinearity (INL) versus code is plotted. The magnitude of the maximum DNL and INL are less than 0.45 and 0.5 LSB, respectively.

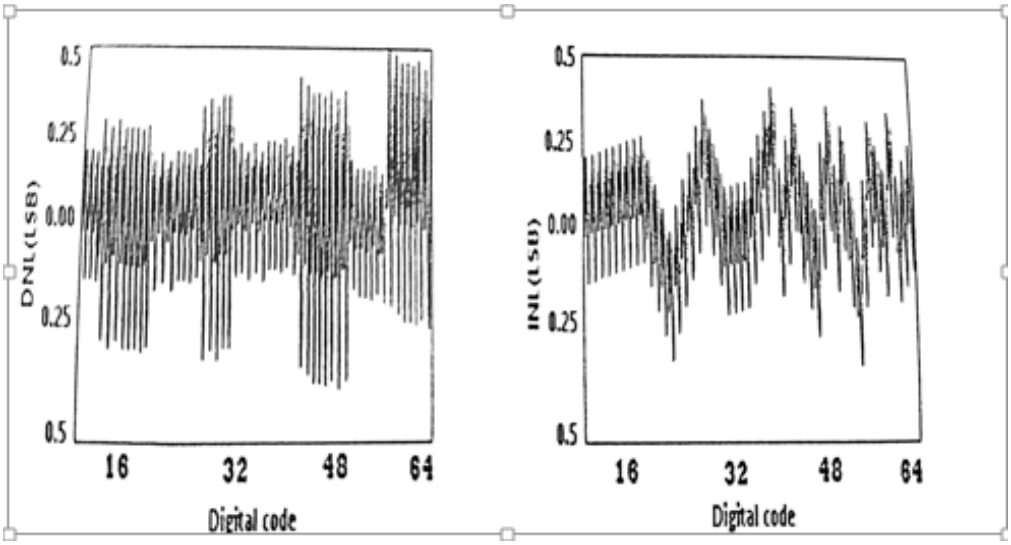

Figure 4(a): Differential Non Linearity (DNL) Versus Code

Figure 4(a): Integral Non Linearity (INL) Versus Code

6. CONCLUSION

In this paper, a new architecture for Analog to Digital conversion is introduced. The proposed scheme reduces number of comparisons required to obtain digital data, which makes the quantization feasible with much higher speed, demonstrating the proposed architecture is effective. Simulation software for mixed circuit is not available, hence an hardwired 8 bit prototype ADC is fabricated and tested.

CONFLICT OF INTERESTS

None

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None

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Datasheet of Intel Microprocessor 8085.

PPI 8255 data sheet